USPIIIi-OPT Software Manual

Version 1.1 — November 2008
Version Revision History

Version 1.1................................................................................................................. November 2008

- Added reference to “2P2 PMC Carrier Board” for clarity to themis-switch-value in Table 2-3, page 2-3, Chapter 2, "USPIIIi-OPT Software".
- Added the section 2.3.1, “Updating from the Recovery OBP”, to Chapter 2, "USPIIIi-OPT Software".
- Changed therm-limit and high-limit temperature thresholds in section 4.2.1, “Setting Temperature Thresholds”, of Chapter 4, "Device Monitoring".
- Made assorted minor revisions and corrections.

Version 1.0................................................................................................................. September 2003
# Table of Contents

How to Use This Manual ........................................................................................................... ix

1. **USPIIIi-OPT Programming Guide** ............................................................................. 1-1
   1.1 Introduction ............................................................................................................ 1-1
   1.2 Jbus address map ................................................................................................... 1-2
   1.3 I2C Bus Topology ............................................................................................... 1-5
   1.4 I2C Devices Address Map ..................................................................................... 1-6
   1.5 The FPGA ............................................................................................................ 1-11
      1.5.1 FPGA Registers (I2C Port 0x3a) ............................................................. 1-11
   1.6 Universe II VME Interface Registers ................................................................. 1-12

2. **USPIIIi-OPT Software** ............................................................................................. 2-1
   2.1 Sun OBP (OpenBoot PROM) Commands ............................................................. 2-1
      2.1.1 Themis-Specific OBP Commands ............................................................. 2-1
      2.1.2 Support Commands .................................................................................... 2-2
         2.1.2.1 probe-scsi-all ............................................................................... 2-2
      2.1.3 USPIIIi-OPT OBP Device aliases ............................................................. 2-2
   2.2 OBP Environment Variables ................................................................................. 2-3
      2.2.1 Themis-Specific OBP Environment Variables .......................................... 2-3
   2.3 Updating the System Flash PROM ........................................................................ 2-5
      2.3.1 Updating from the Recovery OBP ............................................................. 2-6
   2.4 SUN Solaris ........................................................................................................... 2-7
      2.4.1 Environmental Monitoring Programs ....................................................... 2-7

3. **Field-Programmable Gate Array (FPGA)** ............................................................. 3-1
   3.1 FPGA Function Upgrade ..................................................................................... 3-1
      3.1.1 Examples .................................................................................................... 3-2
   3.2 FPGA Register Set ............................................................................................... 3-3
4. Device Monitoring ............................................................................................................ 4-1
  4.1 Introduction ............................................................................................................ 4-1
  4.2 Thermal Monitoring ............................................................................................... 4-1
    4.2.1 Setting Temperature Thresholds ................................................................ 4-4
  4.3 Voltage Monitoring ................................................................................................. 4-8

Index............................................................................................................................. Index-1
List of Figures

Figure 1-1 Jbus Address Space Mapping to PCI Configuration Space 1-4
Figure 1-2 I2C Bus Topology 1-5
Figure 1-3 UCSR Access Mechanism 1-12
Figure 4-1 Placement of USPIIIi-OPT Device Monitors 4-2
Figure 4-2 Outputs of the Temperature Sensor Controller 4-3

List of Tables

Table 1-1 Jbus ID assignment 1-3
Table 1-2 Jbus Address Map 1-3
Table 1-3 USPIIIi-OPT I2C Devices 1-6
Table 1-4 Universe II Register Map 1-13
Table 2-1 Themis-Specific OBP Command 2-2
Table 2-2 List of OBP Aliases 2-2
Table 2-3 Themis-Specific OBP Environment Variables 2-3
Table 2-4 Temperature Monitoring Commands 2-7
Table 2-5 Voltage Monitoring Command 2-8
Table 2-6 User Status LED Commands 2-8
Table 4-1 Voltages Monitored on the CPU-0 and CPU-1 Boards 4-8
Introduction

The Themis Computer USPIIIi-OPT is an UltraSPARC-IIIi-based single-board computer (see photo below) that is SPARC version 9.0 compliant with a VMEbus interface. The software interface for the VMEbus and other on-board peripheral devices is transparently implemented under Solaris. Themis Computer has also developed custom software that enables software programmers to effectively use the powerful features of the VMEbus Interface.
The USPIIIi-OPT has a total of seven models (see Table 1). All models are based on a combination of six different VME boards: the USPIIIi-OPT System board, two CPU boards (CPU-0 and CPU-1), the TGA3D/3D+ Graphics board, and two PMC Carrier boards (one with 2 PMC slots and one with 3 PMC slots).

In addition, a VME-backplane-connected USPIIIi-OPT Paddle Board is available to provide limited I/O connections through the P2 backplane connector (for details, see the USPIIIi-OPT Hardware Manual [Themis P/N 111165-022]).

The USPIIIi-OPT Hardware Manual also provides information on the hardware design of the USPIIIi-OPT system, including a product overview, device monitoring, connector pinouts, jumper-pin and solder-bead configurations, circuit-board and front-panel diagrams, LED interpretation, and VME-slot configurations.

Table 1. USPIIIi-OPT Model Configurations

<table>
<thead>
<tr>
<th>Model /Configuration</th>
<th>CPU-1</th>
<th>CPU-0</th>
<th>System Board</th>
<th>TGA3D/3D+ Graphics Board</th>
<th>PMC Carrier Board (1 only)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>VME Slot 1</td>
<td>VME Slot 2</td>
<td>VME Slot 3</td>
</tr>
<tr>
<td>USPIIIi-OPT/1-2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>USPIIIi-OPT/2G-2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>USPIIIi-OPT/3G2-2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>USPIIIi-OPT/3GP2-2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>USPIIIi-OPT/3GP3-2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>USPIIIi-OPT/2P2-2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>USPIIIi-OPT/2P3-2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td>Yes</td>
</tr>
</tbody>
</table>
Intended Audience

The custom software containing programs, documentation, and packaging, is targeted for various software users:

- System Administrators who install the software and perform the necessary software configuration.
- Users who perform day-to-day operations on USPIIIi-OPT systems.
- Application programmers who write user-level programs to access the VMEbus interface devices through the built-in VMEbus devices.
- System programmers/device-driver writers who develop kernel-level device drivers for VMEbus devices.

Some functions overlap one another. The basic concepts required for many of these functions are common. This manual is structured around the basic concepts of using a VMEbus system.

In Case Of Difficulties

If the USPIIIi-OPT does not behave as described or if you encounter difficulties installing or configuring the board, please call Themis Computer technical support at +1 (510) 252-0870, fax your questions to +1 (510) 490-5529, or e-mail to support@themis.com. You can also contact us via our web site: http://www.themis.com.

UNIX Commands

This document may not contain information on basic UNIX® commands and procedures such as shutting down the system, booting the system, and configuring devices.

See one or more of the following for this information:

- Solaris Handbook for Sun Peripherals, which contains Solaris™ software commands
• *A Practical Guide to Solaris*, Copyright 1999, Mark G. Sobell
• AnswerBook™ on-line documentation for the Solaris software environment
• Other software documentation that you received with your system

### Shell Prompts

<table>
<thead>
<tr>
<th>Shell</th>
<th>Prompt</th>
</tr>
</thead>
<tbody>
<tr>
<td>C shell</td>
<td><em>machine_name</em>%</td>
</tr>
<tr>
<td>C shell superuser</td>
<td><em>machine_name</em>#</td>
</tr>
<tr>
<td>Bourne shell and Korn shell</td>
<td>$</td>
</tr>
<tr>
<td>Bourne shell and Korn shell superuser</td>
<td>#</td>
</tr>
</tbody>
</table>

### Website Information


### Notes, Cautions, Warnings, and Sidebars

The following icons and formatted text are included in this document for the reasons described:

**Note:** A note provides additional information concerning the procedure or action being described that may be helpful in carrying out the procedure or action.
Caution: A caution describes a procedure or action that may result in injury to the operator or equipment damage. This may involve—but is not restricted to—heavy equipment or sharp objects. To reduce the risk, follow the instructions accompanying this symbol.

Warning: A warning describes a procedure or action that may cause injury to the operator or equipment as a result of hazardous voltages. To reduce the risk of electrical shock and danger, follow the instructions accompanying this symbol.

Sidebar: A “sidebar” adds detail to the section within which it is placed, but is not absolutely vital to the description or procedure of the section.

Your Comments are Welcome

We are interested in improving our documentation and welcome your comments and suggestions. You can email your comments to us at docfeedback@themis.com. Please include the document part number in the subject line of your email.
1.1 Introduction

This document provides critical information for software programmers who must write the firmware code to control the extra hardware features implemented on the USPIIIi-OPT. The native firmware from Sun was also modified by Themis to accommodate the topology differences between the Sun reference platform (the Sun Blade 2500 workstation) and the Themis USPIIIi-OPT.

The following is a list of features implemented on the USPIIIi-OPT:

- User 8MB flash memory (AMD device AM29LV065D)
- User LED I²C driver
- Analog voltage I²C converter
- An additional I²C thermal sensor ADM1031 dedicated to the second CPU board temperature monitoring.
- Dual fiber-channel controller ISP2312.
- VME interface based on the Universe-II controller
- USPIIIi-OPT specific control/status registers implemented into a CY37512 programmable logic device from Cypress.
- H/W read/modify write (or test and set) semaphores for shared resources.
Themis modifications include:

- PCI segments topology and its IDsel assignments
- Interrupt assignment/mapping, which impacts the Tomatillo initialization
- I²C bus topology and its address map
- Jbus topology (although it will be transparent to the firmware/software)

1.2 Jbus address map

The Jbus has several agents. Each has its own Agent ID (JID) number, which is used in the decoding process. The Jbus address space has 43 address bits, or 8 Terabytes of address reach. This space is broken up into two 42-bit physical spaces, one for the memory space (cacheable), the other for the IO space (non-cacheable).

<table>
<thead>
<tr>
<th>Main Memory 4TB</th>
<th>0x000.0000.0000</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>includes 16GB for CPU0 cacheable memory space</td>
</tr>
<tr>
<td></td>
<td>includes 16GB for CPU1 cacheable memory space</td>
</tr>
<tr>
<td>I/O space 4TB</td>
<td>0x400.0000.0000</td>
</tr>
<tr>
<td></td>
<td>includes Jbus device configuration space</td>
</tr>
<tr>
<td></td>
<td>PCI address spaces (Cfg/IO/Mem)</td>
</tr>
<tr>
<td></td>
<td>0x800.0000.0000</td>
</tr>
</tbody>
</table>

Each agent on Jbus has its own 5-bit Jbus ID. It has 8 MB of non-cacheable address space assigned for its Jbus configuration registers. These 8 MB windows are defined by:

- \( \text{PA}[42:41] = 10b \)
- \( \text{PA}[40:28] = 0.0000.0000.0000b \)
- \( \text{PA}[27:23] = \text{JID}[4:0] \)
- \( \text{PA}[22:00] = 8\text{MB for Jbus device configuration registers.} \)
Each Jbus agent has its own specific Jbus configuration space layout. The table below provides the layout for the Tomatillo.

Table 1-1. Jbus ID assignment

<table>
<thead>
<tr>
<th>Jbus Agent</th>
<th>JID[4..0]</th>
<th>JbusCfg space</th>
<th>Start address</th>
<th>End address</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jalapeno CPU0</td>
<td>0x00</td>
<td>0x400.0000.0000</td>
<td>0x400.007f.ffff</td>
<td>8MB</td>
<td></td>
</tr>
<tr>
<td>Jalapeno CPU1</td>
<td>0x01</td>
<td>0x400.0080.0000</td>
<td>0x400.00ff.ffff</td>
<td>8MB</td>
<td></td>
</tr>
<tr>
<td>Jalapeno CPU2</td>
<td>0x02</td>
<td>0x400.0100.0000</td>
<td>0x400.017f.ffff</td>
<td>8MB</td>
<td></td>
</tr>
<tr>
<td>Jalapeno CPU3</td>
<td>0x03</td>
<td>0x400.0180.0000</td>
<td>0x400.01ff.ffff</td>
<td>8MB</td>
<td></td>
</tr>
<tr>
<td>Habaniero</td>
<td>0x08</td>
<td>0x400.0400.0000</td>
<td>0x400.047f.ffff</td>
<td>8MB</td>
<td></td>
</tr>
<tr>
<td>Tomatillo 0 (Slave)</td>
<td>0x1c</td>
<td>0x400.0e00.0000</td>
<td>0x400.0e7f.ffff</td>
<td>8MB</td>
<td></td>
</tr>
<tr>
<td>Tomatillo 1 (Master)</td>
<td>0x1e</td>
<td>0x400.0f00.0000</td>
<td>0x400.0f7f.ffff</td>
<td>8MB</td>
<td></td>
</tr>
</tbody>
</table>

Table 1-2. Jbus Address Map

<table>
<thead>
<tr>
<th>Register</th>
<th>add to Jbus cfg base</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jbus Tomatillo ID register</td>
<td>0x0000.0000</td>
</tr>
<tr>
<td>UPA0 offset base register</td>
<td>0x0040.0000</td>
</tr>
<tr>
<td>UPA0 offset mask register</td>
<td>0x0040.0008</td>
</tr>
<tr>
<td>UPA1 offset base register</td>
<td>0x0040.0010</td>
</tr>
<tr>
<td>UPA1 offset mask register</td>
<td>0x0040.0018</td>
</tr>
<tr>
<td>PCI-A Memory offset base register</td>
<td>0x0040.0040</td>
</tr>
<tr>
<td>PCI-A Memory offset mask register</td>
<td>0x0040.0048</td>
</tr>
<tr>
<td>PCI-A Cfg offset base register</td>
<td>0x0040.0050</td>
</tr>
<tr>
<td>PCI-A Cfg offset mask register</td>
<td>0x0040.0058</td>
</tr>
<tr>
<td>PCI-B Memory offset base register</td>
<td>0x0040.0060</td>
</tr>
<tr>
<td>PCI-B Memory offset mask register</td>
<td>0x0040.0068</td>
</tr>
<tr>
<td>PCI-B Cfg offset base register</td>
<td>0x0040.0070</td>
</tr>
<tr>
<td>PCI-B Cfg offset mask register</td>
<td>0x0040.0078</td>
</tr>
<tr>
<td>Tomatillo CSR</td>
<td>0x0041.0000</td>
</tr>
<tr>
<td>PCI-A CSR base register</td>
<td>0x0050.0000</td>
</tr>
<tr>
<td>PCI-B CSR base register</td>
<td>0x0060.0000</td>
</tr>
<tr>
<td>Ichip CSR base register</td>
<td>0x0078.0000</td>
</tr>
</tbody>
</table>
**Figure 1-1.** Jbus Address Space Mapping to PCI Configuration Space
1.3 I\(^2\)C Bus Topology

The USPIII-OPT has several I\(^2\)C busses, numbered 1 to 11. Their topology is provided in Figure 1-2.
1.4 I^2C Devices Address Map

The following table lists all I^2C devices on the USPIIIi-OPT and provides relevant setting information for each of them.

<table>
<thead>
<tr>
<th>Board</th>
<th>Device</th>
<th>I^2C Bus #</th>
<th>HW Physical Address</th>
<th>SW Virtual Address</th>
<th>I^2C Controller with Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>System</td>
<td>ADM1031</td>
<td>I^2C_1</td>
<td>0x58</td>
<td>0x58</td>
<td>I^2C controller: PCF8584 on Xbus</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Temperature monitoring on the system board.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• Therm output used for the thermal interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D1 = Sys board air exhaust temperature</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D2 = Sys board air intake temperature</td>
</tr>
<tr>
<td>System</td>
<td>ICS951601</td>
<td>I^2C_1</td>
<td>0xD2</td>
<td>0xD2</td>
<td>I^2C controller: PCF8584 on Xbus</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• PCI clock generator.</td>
</tr>
<tr>
<td>System</td>
<td>AT24C64</td>
<td>I^2C_1</td>
<td>0xA2 0xAA</td>
<td>0xA2 0xAA</td>
<td>I^2C controller: PCF8584 on Xbus</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• FRU of the USPIIIi-OPT board set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• The content is fully defined by Sun.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 0xAA is an alternate address controlled by the FPGA but not used on the USPIIIi-OPT</td>
</tr>
<tr>
<td>System</td>
<td>FLEX10K30 USPIIIi-OPT (registers)</td>
<td>I^2C_1</td>
<td>0x3A</td>
<td>0x3A</td>
<td>I^2C controller: PCF8584 on Xbus</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• The FPGA of the USPIIIi-OPT is accessed thru the I2C interface. It has two I2C addresses:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>One for the internal FPGA register and the other for the User flash attached to the FPGA I2C/ISA bridge.</td>
</tr>
<tr>
<td>System</td>
<td>FLEX10K30 USPIIIi-OPT (User flash)</td>
<td>I^2C_1</td>
<td>0x38</td>
<td>0x38</td>
<td>I^2C controller: PCF8584 on Xbus</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• The FPGA of the USPIIIi-OPT is accessed thru the I2C interface. It has two I2C addresses:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>One for the internal FPGA register and the other for the User flash attached to the FPGA I2C/ISA bridge.</td>
</tr>
<tr>
<td>Board</td>
<td>Device</td>
<td>I²C Bus #</td>
<td>HW Physical Address</td>
<td>SW Virtual Address</td>
<td>I²C Controller with Description</td>
</tr>
<tr>
<td>-------</td>
<td>----------</td>
<td>-----------</td>
<td>---------------------</td>
<td>--------------------</td>
<td>--------------------------------------------------------------------------------------------------</td>
</tr>
</tbody>
</table>
| System| GBIC GBE1| I2C_8     | 0xA2               | 0xA2              | I²C controller: Southbridge I2C port  
  • The GBIC GBE1 is controlled by the SB I2C port (I2C-7) which is routed thru the FPGA to I2C-8. The register in the FPGA controls the routing of I2C-7 to I2C-8. |
| System| GBIC GBE2| I2C_9     | 0xA2               | 0xA2              | I²C controller: Southbridge I2C port  
  • The GBIC GBE2 is controlled by the SB I2C port (I2C-7) which is routed thru the FPGA to I2C-9. The register in the FPGA controls the routing of I2C-7 to I2C-9. |
| System| GBIC FC1 | I2C_10    | 0xA2               | 0xA2              | I²C controller: Southbridge I2C port  
  • The GBIC FC1 is controlled by the SB I2C port (I2C-7) which is routed thru the FPGA to I2C-10. The register in the FPGA controls the routing of I2C-7 to I2C-10. |
| System| GBIC FC2 | I2C_11    | 0xA2               | 0xA2              | I²C controller: Southbridge I2C port  
  • The GBIC FC2 is controlled by the SB I2C port (I2C-7) which is routed thru the FPGA to I2C-11. The register in the FPGA controls the routing of I2C-7 to I2C-11. |
| CPU-0 | 87LPC764 | I2C_1     | 0x12               | 0x12              | I²C controller: PCF8584 on Xbus  
  • IMAX I2C to I2C bus expander.  
  • The I2C_1 bus is fanned out into 4 additional I2C bus (I2C_2 on Port 0, I2C_3 on Port 1, I2C_4 on Port 2, I2C_5 on Port 3) |
| CPU-0 | ADM1031  | I2C_2     | 0x58               | 0x5C              | I²C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
  • I2C_2 bus is attached to Port #0 of Imax  
  • Temperature monitoring on the CPU0 board  
  Diode D1 = CPU0 die  
  Diode D2 = CPU0 reference Temp1 |

Table 1-3. USPIII-OPT I²C Devices (Continued)
### Table 1-3. USPIII-OPT I2C Devices (Continued)

<table>
<thead>
<tr>
<th>Board</th>
<th>Device</th>
<th>I2C Bus #</th>
<th>HW Physical Address</th>
<th>SW Virtual Address</th>
<th>I2C Controller with Description</th>
</tr>
</thead>
</table>
| CPU-0  | PCF8591     | I2C_4     | 0x90                | 0x90              | I2C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
|        |             |           |                     |                   | *I2C_4 bus is attached to Port #2 of Imax*  
|        |             |           |                     |                   | *DC/DC voltage monitoring on CPU0*  
|        |             |           |                     |                   | - AIN0 -> VCC (Vme backplane)  
|        |             |           |                     |                   | - AIN1 -> 2.5V (DDR voltage)  
|        |             |           |                     |                   | - AIN2 -> 1.5V (Jbus voltage)  
|        |             |           |                     |                   | - AIN3 -> VCCP0 (CPU0 core voltage)  
|        |             |           |                     |                   | Vref = VCC backplane on rev X PCB |
| CPU-0  | AT24C64     | I2C_4     | 0xA4                | 0xD4              | I2C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
|        |             |           |                     |                   | *I2C_4 bus is attached to Port #2 of Imax*  
|        |             |           |                     |                   | *FRU of the USPIII-OPT-CPU0 board set (new revision) to store the Serial number of the CPU0 sub-assembly.* |
| CPU-0  | PCF8574     | I2C_4     | 0x40                | 0x40              | I2C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
|        |             |           |                     |                   | *I2C_4 bus is attached to Port #2 of Imax*  
|        |             |           |                     |                   | Control of User LEDs  
|        |             |           |                     |                   | - P0 -> User Led 0  
|        |             |           |                     |                   | - P1 -> User Led1  
|        |             |           |                     |                   | - P2 -> User Led2  
|        |             |           |                     |                   | - P3 -> User Led3  
|        |             |           |                     |                   | - P4 to P7 return the PCB rev number  
|        |             |           |                     |                   | Code 1111 means rev X  
|        |             |           |                     |                   | Other codes not defined yet. |
| CPU-0  | AT24C64     | I2C_6     | 0xAE                | 0xAE              | Tomatillo Master  
|        |             |           |                     |                   | *USPIII-OPT system parameters stored in EE-prom.* |
| CPU-0  | MC12430     | Pseudo    | Pseudo              | Pseudo            | Tomatillo Slave + FPGA  
|        |             |           |                     |                   | *Jbus clock generator. This is a pseudo I2C bus.* |
### Table 1-3. USPIii-OPT I²C Devices (Continued)

<table>
<thead>
<tr>
<th>Board</th>
<th>Device</th>
<th>I²C Bus #</th>
<th>HW Physical Address</th>
<th>SW Virtual Address</th>
<th>I²C Controller with Description</th>
</tr>
</thead>
</table>
| Memory 0    | 24LCS52| I2C_2     | 0xA0 0x60           | 0xB6 Unmap         | I²C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
• I2C_2 bus is attached to Port #0 of Imax  
• DDR DIMM Eeprom SDF (1st DIMM)                                                                 |
| Memory 0    | 24LCS52| I2C_2     | 0xA2 0x62           | 0xB8 Unmap         | I²C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
• I2C_2 bus is attached to Port #0 of Imax  
• DDR DIMM Eeprom SDF (2nd DIMM)                                                                 |
| Memory 0    | 24LCS52| I2C_2     | 0xA4 0x64           | 0xBA Unmap         | I²C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
• I2C_2 bus is attached to Port #0 of Imax  
• DDR DIMM Eeprom SDF (3rd DIMM)                                                                 |
| Memory 0    | 24LCS52| I2C_2     | 0xA6 0x66           | 0xBC Unmap         | I²C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
• I2C_2 bus is attached to Port #0 of Imax  
• DDR DIMM Eeprom SDF (4th DIMM)                                                                 |
| CPU-1       | ADM1031| I2C_3     | 0x5A                | 0x5E               | I²C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
• I2C_3 bus is attached to Port #1 of Imax  
Temperature monitoring on the CPU1 board  
Diode D1 = CPU1 die  
Diode D2 = CPU1 reference Temp2                                                                 |
| CPU-1       | PCF8591| I2C_3     | 0x92                | 0x92               | I²C controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
• I2C_3 bus is attached to Port #1 of Imax  
DC/DC voltage monitoring on CPU1  
- AIN0 -> VCC (Vme backplane)  
- AIN1 -> 2.5V (DDR voltage)  
- AIN2 -> 1.5V (Jbus voltage)  
- AIN3 -> VCCP1 (CPU1 core voltage)  
Vref = VCC backplane on rev X PCB                                                      |
### Table 1-3. USPIIIi-OPT $I^2C$ Devices (Continued)

<table>
<thead>
<tr>
<th>Board</th>
<th>Device</th>
<th>$I^2C$ Bus #</th>
<th>HW Physical Address</th>
<th>SW Virtual Address</th>
<th>$I^2C$ Controller with Description</th>
</tr>
</thead>
</table>
| CPU-1      | AT24C64    | I2C_3        | 0xAE 0xCE           |                    | $I^2C$ controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
|            |            |              |                     |                    | • I2C_3 bus is attached to Port #1 of Imax  
|            |            |              |                     |                    | • FRU of the USPIIIi-OPT-CPU1 board set (new revision) to store the Serial number of the CPU1 sub-assembly. |
| Memory 1   | 24LCS52    | I2C_3        | 0xA0 0x60           | 0xC6 Unmap         | $I^2C$ controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
|            |            |              |                     |                    | • I2C_3 bus is attached to Port #1 of Imax  
|            |            |              |                     |                    | • DDR DIMM Eeprom SDF (1st DIMM)                                                   |
| Memory 1   | 24LCS52    | I2C_3        | 0xA2 0x62           | 0xC8 Unmap         | $I^2C$ controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
|            |            |              |                     |                    | • I2C_3 bus is attached to Port #1 of Imax  
|            |            |              |                     |                    | • DDR DIMM Eeprom SDF (2nd DIMM)                                                   |
| Memory 1   | 24LCS52    | I2C_3        | 0xA4 0x64           | 0xCA Unmap         | $I^2C$ controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
|            |            |              |                     |                    | • I2C_3 bus is attached to Port #1 of Imax  
|            |            |              |                     |                    | • DDR DIMM Eeprom SDF (3rd DIMM)                                                   |
| Memory 1   | 24LCS52    | I2C_3        | 0xA6 0x66           | 0xCC Unmap         | $I^2C$ controller: PCF8584 on Xbus and IMAX I2C to I2C bus expander  
|            |            |              |                     |                    | • I2C_3 bus is attached to Port #1 of Imax  
|            |            |              |                     |                    | • DDR DIMM Eeprom SDF (4th DIMM)                                                   |

The $I^2C$-to-$I^2C$ bridge expander (Imax) is a microcontroller located on the CPU-0 board, which fans out to the main primary $I^2C$ bus (called I2C_1 in this document) in four secondary $I^2C$ busses designated I2C_2 to I2C_5. These $I^2C$ bus are attached to Ports 0 to 3 respectively of the Imax bridge. The Imax is itself an $I^2C$ device, programmed by OBP through the Xbus-to-$I^2C$ bridge controlled by the Southbridge ASIC on the system board (see $I^2C$ bus topology in Figure 1-2, page 1-5). The $I^2C$ address of the Imax is 0x12.

All the programming details are provided by Sun in two documents. These documents are:
Because of the change on the I²C topology and the additional devices, the address filter bitmap, the routing table, and the address translation page table in the Imax must be modified at the OBP level.

The I²C_7 bus is controlled by the Southbridge device. On the Sun platform, this I²C bus is used to control the SMB card, and is routed to either the GBIC GBE1 or GBE2 or FC1 or FC2. The routing is controlled by a register implemented into the FPGA itself. Before any GBIC I²C device is accessed, the software is responsible for setting this register accordingly.

1.5 The FPGA

The Field-Programmable Gate Array (FPGA) is a multi-functional device with various registers used to control many different functions of the USPIIIi-OPT. It includes miscellaneous control logic and an I²C-to-Ebus bridge to access the user Flash PROM (AMD 29LV065). The control logic is accessed through a set of FPGA registers from I²C port address 0x3a; the user Flash is accessed through I²C port address 0x38.

1.5.1 FPGA Registers (I²C Port 0x3a)

See Chapter 3, "Field-Programmable Gate Array (FPGA)", for a full description of the FPGA registers.
1.6 Universe II VME Interface Registers

The Universe II Control and Status Registers facilitate host system configuration and allow the user to control Universe II operational characteristics. The registers are divided into the following groups:

- VMEbus Configuration and Status Registers
- Universe II Device Specific Status Registers
  —The Universe II registers have little-endian byte-ordering
- PCI Configuration Space

A Universe-II register map is shown in Table 1-4 on page 1-13.

![Figure 1-3. UCSR Access Mechanism](image-url)
### Table 1-4. Universe II Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>PCI Configuration Space ID Register</td>
<td>PCI_ID</td>
</tr>
<tr>
<td>004</td>
<td>PCI Configuration Space Control and Status Register</td>
<td>PCI_CSR</td>
</tr>
<tr>
<td>008</td>
<td>PCI Configuration Class Register</td>
<td>PCI_CLASS</td>
</tr>
<tr>
<td>00C</td>
<td>PCI Configuration Miscellaneous 0 Register</td>
<td>PCI_MISC0</td>
</tr>
<tr>
<td>010</td>
<td>PCI Configuration Base Address 0 Register</td>
<td>PCI_BS0</td>
</tr>
<tr>
<td>014</td>
<td>PCI Configuration Base Address 1 Register</td>
<td>PCI_BS1</td>
</tr>
<tr>
<td>018-024</td>
<td>PCI Unimplemented</td>
<td></td>
</tr>
<tr>
<td>028</td>
<td>PCI Reserved</td>
<td></td>
</tr>
<tr>
<td>02C</td>
<td>PCI Reserved</td>
<td></td>
</tr>
<tr>
<td>030</td>
<td>PCI Unimplemented</td>
<td></td>
</tr>
<tr>
<td>034</td>
<td>PCI Reserved</td>
<td></td>
</tr>
<tr>
<td>038</td>
<td>PCI Reserved</td>
<td></td>
</tr>
<tr>
<td>03C</td>
<td>PCI Configuration Miscellaneous 1 Register</td>
<td>PCI_MISC1</td>
</tr>
<tr>
<td>040-0FF</td>
<td>PCI Unimplemented</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>PCI Target Image 0 Control Register</td>
<td>LSI0_CTL</td>
</tr>
<tr>
<td>104</td>
<td>PCI Target Image 0 Base Address Register</td>
<td>LSI0_BS</td>
</tr>
<tr>
<td>108</td>
<td>PCI Target Image 0 Bound Address Register</td>
<td>LSI0_BD</td>
</tr>
<tr>
<td>10C</td>
<td>PCI Target Image 0 Translation Offset Register</td>
<td>LSI0_TO</td>
</tr>
<tr>
<td>110</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>114</td>
<td>PCI Target Image 1 Control Register</td>
<td>LSI1_CTL</td>
</tr>
<tr>
<td>118</td>
<td>PCI Target Image 1 Base Address Register</td>
<td>LSI1_BS</td>
</tr>
<tr>
<td>11C</td>
<td>PCI Target Image 1 Bound Address Register</td>
<td>LSI1_BD</td>
</tr>
<tr>
<td>120</td>
<td>PCI Target Image 1 Translation Offset Register</td>
<td>LSI1_TO</td>
</tr>
<tr>
<td>124</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>Offset</td>
<td>Register</td>
<td>Name</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------</td>
<td>---------</td>
</tr>
<tr>
<td>128</td>
<td>PCI Target Image 2 Control Register</td>
<td>LSI2_CTL</td>
</tr>
<tr>
<td>12C</td>
<td>PCI Target Image 2 Base Address Register</td>
<td>LSI2_BS</td>
</tr>
<tr>
<td>130</td>
<td>PCI Target Image 2 Bound Address Register</td>
<td>LSI2_BD</td>
</tr>
<tr>
<td>134</td>
<td>PCI Target Image 2 Translation Offset Register</td>
<td>LSI2_TO</td>
</tr>
<tr>
<td>138</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>13C</td>
<td>PCI Target Image 3 Control Register</td>
<td>LSI3_CTL</td>
</tr>
<tr>
<td>140</td>
<td>PCI Target Image 3 Base Address Register</td>
<td>LSI3_BS</td>
</tr>
<tr>
<td>144</td>
<td>PCI Target Image 3 Bound Address Register</td>
<td>LSI3_BD</td>
</tr>
<tr>
<td>148</td>
<td>PCI Target Image 3 Translation Offset Register</td>
<td>LSI3_TO</td>
</tr>
<tr>
<td>14C-16C</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>170</td>
<td>Special Cycle Control Register</td>
<td>SCYC_CTL</td>
</tr>
<tr>
<td>174</td>
<td>Special Cycle PCI Bus Address Register</td>
<td>SCYC_ADDR</td>
</tr>
<tr>
<td>178</td>
<td>Special Cycle Swap/Compare Enable Register</td>
<td>SCYC_EN</td>
</tr>
<tr>
<td>17C</td>
<td>Special Cycle Compare Data Register</td>
<td>SCYC_CMP</td>
</tr>
<tr>
<td>180</td>
<td>Special Cycle Swap Data Register</td>
<td>SCYC_SWP</td>
</tr>
<tr>
<td>184</td>
<td>PCI miscellaneous Register</td>
<td>LMISC</td>
</tr>
<tr>
<td>188</td>
<td>Special PCI Target Image Register</td>
<td>SLSI</td>
</tr>
<tr>
<td>18C</td>
<td>PCI command Error Log Register</td>
<td>L_CMDERR</td>
</tr>
<tr>
<td>190</td>
<td>PCI Address Error Log Register</td>
<td>LAERR</td>
</tr>
<tr>
<td>194-19C</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1A0</td>
<td>PCI Target Image 4 Control Register</td>
<td>LSI4_CTL</td>
</tr>
<tr>
<td>1A4</td>
<td>PCI Target Image 4 Base Address Register</td>
<td>LSI4_BS</td>
</tr>
<tr>
<td>1A8</td>
<td>PCI Target Image 4 Bound Address Register</td>
<td>LSI4_BD</td>
</tr>
<tr>
<td>1AC</td>
<td>PCI Target Image 4 Translation Offset Register</td>
<td>LSI4_TO</td>
</tr>
<tr>
<td>1B0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1B4</td>
<td>PCI Target Image 5 Control Register</td>
<td>LSI5_CTL</td>
</tr>
</tbody>
</table>
### Table 1-4. Universe II Register Map (Continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1B8</td>
<td>PCI Target Image 5 Base Address Register</td>
<td>LSI5_BS</td>
</tr>
<tr>
<td>1BC</td>
<td>PCI Target Image 5 Bound Address Register</td>
<td>LSI5_BD</td>
</tr>
<tr>
<td>1C0</td>
<td>PCI Target Image 5 Translation Offset Register</td>
<td>LSI5_TO</td>
</tr>
<tr>
<td>1C4</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1C8</td>
<td>PCI Target Image 6 Control Register</td>
<td>LSI6_CTL</td>
</tr>
<tr>
<td>1CC</td>
<td>PCI Target Image 6 Base Address Register</td>
<td>LSI6_BS</td>
</tr>
<tr>
<td>1D0</td>
<td>PCI Target Image 6 Bound Address Register</td>
<td>LSI6_BD</td>
</tr>
<tr>
<td>1D4</td>
<td>PCI Target Image 6 Translation Offset Register</td>
<td>LSI6_TO</td>
</tr>
<tr>
<td>1D8</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1DC</td>
<td>PCI Target Image 7 Control Register</td>
<td>LSI7_CTL</td>
</tr>
<tr>
<td>1E0</td>
<td>PCI Target Image 7 Base Address Register</td>
<td>LSI7_BS</td>
</tr>
<tr>
<td>1E4</td>
<td>PCI Target Image 7 Bound Address Register</td>
<td>LSI7_BD</td>
</tr>
<tr>
<td>1E8</td>
<td>PCI Target Image 7 Translation Offset Register</td>
<td>LSI7_TO</td>
</tr>
<tr>
<td>1EC-1FC</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td>DMA Transfer Control Register</td>
<td>DCTL</td>
</tr>
<tr>
<td>204</td>
<td>DMA Transfer Byte Count Register</td>
<td>DTBC</td>
</tr>
<tr>
<td>208</td>
<td>DMA PCI Bus Address Register</td>
<td>DLA</td>
</tr>
<tr>
<td>20C</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>210</td>
<td>DMA VMEbus Address Register</td>
<td>DVA</td>
</tr>
<tr>
<td>214</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>218</td>
<td>DMA Command Packet Pointer Register</td>
<td>DCPP</td>
</tr>
<tr>
<td>21C</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>220</td>
<td>DMA General Control and Status Register</td>
<td>DGCS</td>
</tr>
<tr>
<td>224</td>
<td>DMA Linked List Update Enable Register</td>
<td>D_LLUE</td>
</tr>
<tr>
<td>228-2FC</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>300</td>
<td>PCI Interrupt ENABLE Register</td>
<td>LINT_EN</td>
</tr>
<tr>
<td>304</td>
<td>PCI Interrupt Status Register</td>
<td>LINT_STAT</td>
</tr>
<tr>
<td>308</td>
<td>PCI Interrupt Map 0 Register</td>
<td>LINT_MAP0</td>
</tr>
</tbody>
</table>
Table 1-4. Universe II Register Map (Continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>30C</td>
<td>PCI Interrupt Map 1 Register</td>
<td>LINT_MAP1</td>
</tr>
<tr>
<td>320</td>
<td>Interrupt Status/ID Out Register</td>
<td>STATID</td>
</tr>
<tr>
<td>324</td>
<td>VIRQ1 STATUS/ID Register</td>
<td>V1_STATID</td>
</tr>
<tr>
<td>328</td>
<td>VIRQ2 STATUS/ID Register</td>
<td>V2_STATID</td>
</tr>
<tr>
<td>32C</td>
<td>VIRQ3 STATUS/ID Register</td>
<td>V3_STATID</td>
</tr>
<tr>
<td>330</td>
<td>VIRQ4 STATUS/ID Register</td>
<td>V4_STATID</td>
</tr>
<tr>
<td>334</td>
<td>VIRQ5 STATUS/ID Register</td>
<td>V5_STATID</td>
</tr>
<tr>
<td>338</td>
<td>VIRQ6 STATUS/ID Register</td>
<td>V6_STATID</td>
</tr>
<tr>
<td>33C</td>
<td>VIRQ7 STATUS/ID Register</td>
<td>V7_STATID</td>
</tr>
<tr>
<td>340</td>
<td>PCI Interrupt Map 2 Register</td>
<td>LINT_MAP2</td>
</tr>
<tr>
<td>344</td>
<td>VME Interrupt Map 1 Register</td>
<td>VINT_MAP2</td>
</tr>
<tr>
<td>348</td>
<td>Mailbox 0 Register</td>
<td>MBOX0</td>
</tr>
<tr>
<td>34C</td>
<td>Mailbox 1 Register</td>
<td>MBOX1</td>
</tr>
<tr>
<td>350</td>
<td>Mailbox 2 Register</td>
<td>MBOX2</td>
</tr>
<tr>
<td>354</td>
<td>Mailbox 3 Register</td>
<td>MBOX3</td>
</tr>
<tr>
<td>358</td>
<td>Semaphore 0 Register</td>
<td>SEMA0</td>
</tr>
<tr>
<td>35C</td>
<td>Semaphore 1 Register</td>
<td>SEMA1</td>
</tr>
<tr>
<td>360-3FC</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>400</td>
<td>Master Control Register</td>
<td>MAST_CTL</td>
</tr>
<tr>
<td>404</td>
<td>Miscellaneous Control Register</td>
<td>MISC_CTL</td>
</tr>
<tr>
<td>408</td>
<td>Miscellaneous Status Register</td>
<td>MISC_STAT</td>
</tr>
<tr>
<td>40C</td>
<td>User AM Codes Register</td>
<td>USER_AM</td>
</tr>
<tr>
<td>410-EFC</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>F00</td>
<td>VMEbus Slave Image 0 Control Register</td>
<td>VSI0_CTL</td>
</tr>
<tr>
<td>F04</td>
<td>VMEbus Slave Image 0 Base Address Register</td>
<td>VSI0_BS</td>
</tr>
<tr>
<td>F08</td>
<td>VMEbus Slave Image 0 bound Address Register</td>
<td>VSI0_BD</td>
</tr>
<tr>
<td>F0C</td>
<td>VMEbus Slave Image 0 Translation Offset Register</td>
<td>VSI0_TO</td>
</tr>
</tbody>
</table>
### Table 1-4. Universe II Register Map (Continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>F10</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>F14</td>
<td>VMEbus Slave Image 1 Control Register</td>
<td>VSI1_CTL</td>
</tr>
<tr>
<td>F18</td>
<td>VMEbus Slave Image 1 Bound Address Register</td>
<td>VSI1_BS</td>
</tr>
<tr>
<td>F1C</td>
<td>VMEbus Slave Image 1 Bound Address Register</td>
<td>VSI1_BD</td>
</tr>
<tr>
<td>F20</td>
<td>VMEbus Slave Image 1 Translation Offset Register</td>
<td>VSI1_TO</td>
</tr>
<tr>
<td>F24</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>F28</td>
<td>VMEbus Slave Image 2 Control Register</td>
<td>VSI2_CTL</td>
</tr>
<tr>
<td>F2C</td>
<td>VMEbus Slave Image 2 Bound Address Register</td>
<td>VSI2_BS</td>
</tr>
<tr>
<td>F30</td>
<td>VMEbus Slave Image 2 Bound Address Register</td>
<td>VSI2_BD</td>
</tr>
<tr>
<td>F34</td>
<td>VMEbus Slave Image 2 Translation Offset Register</td>
<td>VSI2_TO</td>
</tr>
<tr>
<td>F38</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>F3C</td>
<td>VMEbus Slave Image 3 Control Register</td>
<td>VSI3_CTL</td>
</tr>
<tr>
<td>F40</td>
<td>VMEbus Slave Image 3 Bound Address Register</td>
<td>VSI3_BS</td>
</tr>
<tr>
<td>F44</td>
<td>VMEbus Slave Image 3 Bound Address Register</td>
<td>VSI3_BD</td>
</tr>
<tr>
<td>F48</td>
<td>VMEbus Slave Image 3 Translation Offset Register</td>
<td>VSI3_TO</td>
</tr>
<tr>
<td>F4C-F60</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>F64</td>
<td>Location Monitor Control Register</td>
<td>LM_CTL</td>
</tr>
<tr>
<td>F68</td>
<td>Location Monitor Base Address Register</td>
<td>LM_BS</td>
</tr>
<tr>
<td>F6C</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>F70</td>
<td>VMEbus Register Access Image Control Register</td>
<td>VRAI_CTL</td>
</tr>
<tr>
<td>F74</td>
<td>VMEbus Register Access Image Base Address Register</td>
<td>VRAI_BS</td>
</tr>
<tr>
<td>F78</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>F7C</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>F80</td>
<td>VMEbus CSR Control Register</td>
<td>VCSR_CTL</td>
</tr>
<tr>
<td>F84</td>
<td>VMEbus CSR Translation Offset Register</td>
<td>VSCR_TO</td>
</tr>
</tbody>
</table>
### Table 1-4. Universe II Register Map (Continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>F88</td>
<td>VMEbus AM Code Error Log Register</td>
<td>V_AMERR</td>
</tr>
<tr>
<td>F8C</td>
<td>VMEbus Address Error Log Register</td>
<td>VAERR</td>
</tr>
<tr>
<td>F90</td>
<td>VMEbus Slave Image 4 Control Register</td>
<td>VSI4_CTL</td>
</tr>
<tr>
<td>F94</td>
<td>VMEbus Slave Image 4 Bound Address Register</td>
<td>VSI4_BS</td>
</tr>
<tr>
<td>F98</td>
<td>VMEbus Slave Image 4 Bound Address Register</td>
<td>VSI4_BD</td>
</tr>
<tr>
<td>F9C</td>
<td>VMEbus Slave Image 4 Translation Offset Register</td>
<td>VSI4_TO</td>
</tr>
<tr>
<td>FA0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>FA4</td>
<td>VMEbus Slave Image 5 Control Register</td>
<td>VSI5_CTL</td>
</tr>
<tr>
<td>FA8</td>
<td>VMEbus Slave Image 5 Bound Address Register</td>
<td>VSI5_BS</td>
</tr>
<tr>
<td>FAC</td>
<td>VMEbus Slave Image 5 Bound Address Register</td>
<td>VSI5_BD</td>
</tr>
<tr>
<td>FB0</td>
<td>VMEbus Slave Image 5 Translation Offset Register</td>
<td>VSI5_TO</td>
</tr>
<tr>
<td>FB4</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>FB8</td>
<td>VMEbus Slave Image 6 Control Register</td>
<td>VSI6_CTL</td>
</tr>
<tr>
<td>FBC</td>
<td>VMEbus Slave Image 6 Bound Address Register</td>
<td>VSI6_BS</td>
</tr>
<tr>
<td>FC0</td>
<td>VMEbus Slave Image 6 Bound Address Register</td>
<td>VSI6_BD</td>
</tr>
<tr>
<td>FC4</td>
<td>VMEbus Slave Image 6 Translation Offset Register</td>
<td>VSI6_TO</td>
</tr>
<tr>
<td>FC8</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>FCC</td>
<td>VMEbus Slave Image 7 Control Register</td>
<td>VSI7_CTL</td>
</tr>
<tr>
<td>FD0</td>
<td>VMEbus Slave Image 7 Bound Address Register</td>
<td>VSI7_BS</td>
</tr>
<tr>
<td>FD4</td>
<td>VMEbus Slave Image 7 Bound Address Register</td>
<td>VSI7_BD</td>
</tr>
<tr>
<td>FD8</td>
<td>VMEbus Slave Image 7 Translation Offset Register</td>
<td>VSI7_TO</td>
</tr>
<tr>
<td>FDC-FEC</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>FF0</td>
<td>VME CR/CSR Reserved</td>
<td></td>
</tr>
<tr>
<td>FF4</td>
<td>VMEbus CSR Bit Clear Register</td>
<td>VCSR_CLR</td>
</tr>
<tr>
<td>FF8</td>
<td>VMEbus CSR Bit Set Register</td>
<td>VCSR_SET</td>
</tr>
<tr>
<td>FFC</td>
<td>VMEbus CSR Address Register</td>
<td>VCSR_BS</td>
</tr>
</tbody>
</table>
USPIIIi-OPT Software

2.1 Sun OBP (OpenBoot PROM) Commands

The USPIIIi-OPT incorporates Sun's standard OBP version 4.9.0 and higher as the default firmware. In addition, Themis has added specific OBP functions to support the additional Fibre Channel, dual Optical Ethernet interfaces, the Themis FPGA device, and the VME interface.

2.1.1 Themis-Specific OBP Commands

Several OBP command extensions are specific to the USPIIIi-OPT. All other OBP commands are the same as the Sun UltraSPARC-IIIi platform. Specific details of the OBP architecture are defined in the IEEE 1275 specification document.

Reference materials that describe the OBP include:

- OpenBoot 4.x Command Reference -- Sun Part Number: 816-1177-10
- OpenBoot Quick Reference -- Sun Part Number: 802-5675-31
- Writing FCode 3.1 Programs -- Sun Part Number: 802-3239-31.f3f_

Table 2-1 on page 2-2 lists the Themis-specific OBP commands that are accessible at the OBP “ok” prompt.
### 2.1.2 Support Commands

#### 2.1.2.1 probe-scsi-all

The command `probe-scsi-all` probes the first SCSI bus (SCSI A) and the second SCSI bus (SCSI B). This command behaves in a similar fashion to the standard OBP command `probe-scsi`.

#### 2.1.3 USPIIIi-OPT OBP Device aliases

The `devalias` command displays the list of OBP aliases for the USPIIIi-OPT, as shown in Table 2-2.

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>ok devalias</code></td>
<td></td>
</tr>
<tr>
<td><code>net2</code></td>
<td>/pci@1d,700000/network@2,1</td>
</tr>
<tr>
<td><code>net</code></td>
<td>/pci@1d,700000/network@2</td>
</tr>
<tr>
<td><code>ide</code></td>
<td>/pci@1e,600000/ide@d</td>
</tr>
<tr>
<td><code>cdrom</code></td>
<td>/pci@1d,700000/scsi@4/disk@6,0:f</td>
</tr>
<tr>
<td><code>disk1</code></td>
<td>/pci@1d,700000/scsi@4/disk@1,0</td>
</tr>
<tr>
<td><code>disk0</code></td>
<td>/pci@1d,700000/scsi@4/disk@0,0</td>
</tr>
<tr>
<td><code>disk</code></td>
<td>/pci@1d,700000/scsi@4/disk@0,0</td>
</tr>
<tr>
<td><code>scsi</code></td>
<td>/pci@1d,700000/scsi@4</td>
</tr>
<tr>
<td><code>ttyb</code></td>
<td>/pci@1e,600000/isa@7/serial@0,2e8</td>
</tr>
<tr>
<td><code>ttya</code></td>
<td>/pci@1e,600000/isa@7/serial@0,3f8</td>
</tr>
</tbody>
</table>
2.2 OBP Environment Variables

OBP environment variables (see Table 2-3) may be set at the OBP “ok” prompt by using the setenv command.

```
ok setenv variable_name value
```

When running Solaris, the following command may be used (the syntax may vary depending on the type of command line shell used).

```
# eeprom variable_name=value
```

A board “reset-all” is required for the new values to take effect.

2.2.1 Themis-Specific OBP Environment Variables

Table 2-3 lists the Themis-specific OBP environment variables for the USPIIIi-OPT.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>themis-cpu-count</td>
<td>The number of processors on the system.</td>
</tr>
<tr>
<td>therm-reset-hold</td>
<td>When not disabled (default), this will prevent the system from resetting after a thermal shutdown condition even if the sensor temperature drops below the threshold by 5C.</td>
</tr>
<tr>
<td>Audio-device?</td>
<td>When disabled (default), this will delete the audio device node. Set this variable to &quot;enabled&quot; if you have a paddle board or a PMC Carrier Board (2P2) that supports the AC97 audio interface.</td>
</tr>
<tr>
<td>system-low-limit</td>
<td>The low temperature threshold for the System board, below which the sensor will be in a warning state.</td>
</tr>
<tr>
<td>system-therm-limit</td>
<td>The shutdown temperature threshold for the System board, above which the sensor will assert the THERM signal, causing the system to be held in reset.</td>
</tr>
<tr>
<td>system-high-limit</td>
<td>The high temperature threshold for the System board, above which the sensor will be in a warning state.</td>
</tr>
<tr>
<td>cpu0-low-limit</td>
<td>The low temperature threshold for the CPU0 board, below which the sensor will be in a warning state.</td>
</tr>
<tr>
<td>Variable</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------------</td>
<td>--------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>cpu0-therm-limit</td>
<td>The shutdown temperature threshold for the CPU0 board, above which the sensor will assert the THERM signal, causing the system to be held in reset.</td>
</tr>
<tr>
<td>cpu0-high-limit</td>
<td>The high temperature threshold for the CPU0 board, above which the sensor will be in a warning state.</td>
</tr>
<tr>
<td>cpu1-low-limit</td>
<td>The low temperature threshold for the CPU1 board, below which the sensor will be in a warning state.</td>
</tr>
<tr>
<td>cpu1-therm-limit</td>
<td>The shutdown temperature threshold for the CPU1 board, above which the sensor will assert the THERM signal, causing the system to be held in reset.</td>
</tr>
<tr>
<td>cpu1-high-limit</td>
<td>The high temperature threshold for the CPU1 board, above which the sensor will be in a warning state.</td>
</tr>
<tr>
<td>local-mac-address?</td>
<td>When set to true (default), this enables the second network node to get a local-mac-address value that is &quot;1&quot; greater than the system-mac-address. This variable needs to be true for both network nodes to have their own unique mac addresses during Solaris configuration.</td>
</tr>
<tr>
<td>themis-switch-value</td>
<td>The value corresponding to the front-panel rotary switch setting of the 2P2 PMC Carrier Board; valid values are from 0 through 15.(^a)</td>
</tr>
</tbody>
</table>

\(^a\)—This applies only to the rotary switch of the 2P2 PMC Carrier Board.
2.3 Updating the System Flash PROM

**Warning:** GREAT CARE must be taken when performing a Flash upgrade. If an invalid or corrupted PROM file was downloaded, or if you experience a power outage during the process, the USPIIIi-OPT may not be bootable. DO NOT interrupt the command while it is in progress.

To update the system (boot) flash PROM device:

1. First download the OBP image from the tftpboot server. To do this, type

   4000 dload obpimage-file

   For example,

   {1} ok 4000 dload usp3i_opt.rev1.6
   Boot device: /pci@1f,700000/network@2:,usp3i_opt.rev1.6
   File and args:
   1000 Mbps full-duplex
   Timeout waiting for ARP/RARP packet
   104000
   Server IP address: 198.211.242.2
   Client IP address: 198.211.242.62

2. Next, type the flash-update command to write the OBP image to the flash

   {1} ok flash-update

   which results in:

   Update flash with the downloaded OBP image
   Erasing ... done
   Copying ..
   Verifying ..

   This command writes the previously downloaded OBP image file to flash.

   It is best to update your flash PROM directly after resetting the system.

   Call your Unix system administrator in case of problems.
2.3.1 Updating from the Recovery OBP

To update the system (boot) flash PROM device from the recovery OBP:

1. Place the rotary switch in position E or F or remove the jumper JP2502, then power on the board.

2. Next, download the latest revision of OBP. For example, `4000 dload <OBP long filename with absolute directory path>`. It is important to have the proper tftpboot server setup, as well as a working optical Ethernet connection (bottom gigabit Ethernet port A1 only). For example,

   `{1} ok 4000 dload usp3i_opt.rev1.6
   Boot device: /pci@1f,700000/network@2:,usp3i_opt.rev1.6
   File and args:
   1000 Mbps full-duplex
   Timeout waiting for ARP/RARP packet
   104000
   Server IP address: 198.211.242.2
   Client IP address: 198.211.242.62

3. Point to the lower section of the flash by entering the following command at the OBP ok prompt:

   9 fpgac@ f7 and 9 fpgac!

   **Caution:** This command is essential to updating the boot flash. If the command is not entered as shown, the recovery flash will be updated instead of the boot flash.

   The flash-update command will now point to the lower section of the flash.

4. Next, type the flash-update command to write the OBP image to the flash

   `{1} ok flash-update

   which results in:

   Update flash with the downloaded OBP image
   Erasing ... done
   Copying ..
   Verifying ..

   This command writes the previously downloaded OBP image file to flash.

5. Power off the board, turn the rotary switch to position 0, and insert the jumper JP2502 (if removed).
2.4 SUN Solaris

The USPIIIi-OPT can run the Solaris OS from either a local disk or from the Ethernet network as a diskless client. In the case of a local disk, the Solaris OS will be installed from the Sun Solaris CD-ROM. To install the USPIIIi-OPT as a diskless client, users need to run Sun’s Solstice on a boot server system. Please refer to Sun’s documentation on how to install the Solaris Operating System.

It is also possible to set up a Solaris diskless server without a graphical user interface. Four simple character-based commands are needed, two from the Solaris install CDs (`setup_install_server` and `add_to_install_server`), and two from the server (`smosservice` and `smdiskless`).

2.4.1 Environmental Monitoring Programs

The following Solaris application programs have been written specifically for the USPIIIi-OPT system:

`usp3i_temp`

The `usp3i_temp` application (see Table 2-4) interfaces with the ADM1031 temperature monitors that are installed on the System, CPU0, and CPU1 boards.

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>usp3i_temp</td>
<td>Dumps the temperature and threshold settings</td>
</tr>
<tr>
<td>usp3i_temp -c</td>
<td>This is an interactive method for changing temperature thresholds. This change will remain in effect until the next power cycle. To make permanent threshold values, use the OBP environment variable (see Section 4.2.1, “Setting Temperature Thresholds,” on page 4-4).</td>
</tr>
<tr>
<td>usp3i_temp -m</td>
<td>Causes the system to run in an infinite loop monitoring abnormal conditions and reporting to the console.</td>
</tr>
</tbody>
</table>

`usp3i_voltage`

The `usp3i_voltage` application (see Table 2-5 on page 2-8) interfaces with the PCF8591 device that is used for DC/DC voltage monitoring on both CPU0 and
CPU1.

Table 2-5. Voltage Monitoring Command

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>usp3i_voltage</td>
<td>Dumps all voltages (backplane, memory, Jbus, and CPU core).</td>
</tr>
</tbody>
</table>

usp3i_uled

The usp3i_uled application (see Table 2-6) interfaces with the PCF8574 device on the CPU0 board that controls the four User Status LEDs.

Table 2-6. User Status LED Commands

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>usp3i_uled -e led#</td>
<td>Turns ON the specified User LED (# = 1 through 4).</td>
</tr>
<tr>
<td>usp3i_uled -d led#</td>
<td>Turns OFF the specified User LED (# = 1 through 4).</td>
</tr>
</tbody>
</table>
Field-Programmable Gate Array (FPGA)

The USPIIIi Field-Programmable Gate Array (FPGA) is accessible through the EBus, Xbus, and FC bus and has 16 registers used to control a variety of different functions. These registers are described later in this chapter. Access and control of FPGA registers require a knowledge of FPGA functions (see following section).

The advantage of using the FPGA as opposed to the PLD (Programmable Logic Device) approach used by other Themis systems is that both boot and user flash PROMs may be upgraded in the field without bringing the system down.

3.1 FPGA Function Upgrade

Certain FPGA functions have been added to OBP 3.2 to facilitate the operation and analysis of the USPIIIi system. These include:

- `themis-show-pld` .................................................................Displays a list of all functions
- `dump-fpga` (dump-pld) ..............................Performs an FPGA register dump
- `themis-pld-version` .......................................................Displays the FPGA version
- `dump-jumper` .................................Performs an FPGA jumper and solder-bead dump
- `<offset> fpga@`......................Places SysIO register on OBP stack at offset from base
- `<data> <offset> fpga!` ..............Write data into SysIO register at offset from base

In addition, the following functions are available to read and write FPGA registers directly as a character (c) or byte, word (w), or long word (l):
3.1.1 Examples

The following examples illustrate how a typical function works:

1. Read FPGA register 0x04:

   ok 4 pldc@ . <Enter>

   ok f \ .......................... Bit values returned are [ 0 0 0 0 1 1 1 1 ]

2. Set bit 4 and bit 5 of FPGA register 0x04 to 1:

   ok 3f 4 pldc! <Enter>

3. Verify that bit 4 and bit 5 of FPGA register 0x04 have been set to 1:

   ok 4 pldc@ . <Enter>

   ok 3f \ .......................... Bit values returned are [ 0 0 1 1 1 1 1 1 ]
3.2 FPGA Register Set

The following is extracted from the register descriptions written in the VHDL source code of the FPGA itself.

```
-- FPGA register : offset 0x00
-- Description : FPGA revision and ID
-- Width : 8-bit
-- Vector name : fpga_reg(0,i)

-- Description
-- bits [3..0] : Revision of this FPGA
-- 0xf is reserved for engineering
-- 0x0 is reserved for the recovery FPGA
-- others : current revision level of the FPGA
-- bits [7..4] : CPU family ID
-- 0001 ---> Hummingbird
-- 0010 ---> Phantom
-- 0011 ---> Corsair
-- 0100 ---> CPU 3i

-- FPGA register : offset 0x01
-- Description : User jumper and Boot device jumper
-- Width : 8-bit
-- Vector name : fpga_reg(1,i)

-- Description
-- bit 0 : (RO) - Status of Jumper JP2601
-- 0 : JP2601 jumper is OFF
-- 1 : JP2601 jumper is installed.
-- bit 1 : (RO) - Status of Jumper JP2602
-- 0 : JP2602 jumper is OFF - Boot device is the external Rombo.
-- 1 : JP2602 jumper is installed. - Boot device is the on-board OBP flash.
-- bit 2 : (RO) - Status of Jumper JP2603
-- 0 : JP2603 jumper is OFF - OBP on-board flash is write-protected
-- 1 : JP2603 jumper is installed. - OBP on-board flash is writeable
-- bit 3 : (RO) - Status of Jumper JP2608
-- 0 : JP2608 jumper is OFF - The shutdown condition will force the board under reset
-- 1 : JP2608 jumper is installed. - The shutdown condition will not put the board under reset.(Battle mode)
-- bit 4 : (RO) - Status of the M66en signal for PCI1A. (TGA3D+)
-- 0 : The PCI bus PCI1A is running at 33Mhz
-- 1 : The PCI bus PCI1A is running at 66Mhz
```
-- bit 5 : (RO) - Status of the M66en signal for PCI1B. (SCSI-GBE)
-- 0 : The PCI bus PCI1B is running at 33Mhz
-- 1 : The PCI bus PCI1B is running at 66Mhz
-- bit 6 : (RO) - Status of the M66en signal for PCI2A. (UNIVERSE-ALI)
-- 0 : The PCI bus PCI2A is running at 33Mhz
-- 1 : The PCI bus PCI2A is running at 66Mhz
-- bit 7 : (RO) - Status of the M66en signal for PCI2B. (FC-AL)
-- 0 : The PCI bus PCI2B is running at 33Mhz
-- 1 : The PCI bus PCI2B is running at 66Mhz
-- ----------------------------------
-- FPGA register : offset 0x02
-- Description : VME slot geographical ID
-- Width : 8-bit
-- Vector name : fpga_reg(2,i)
-- ----------------------------------
-- Description
-- bit 0 : (RO) - Status of VME P1 signal GA0 (pin P1.D10)
-- 0 : GA0 pull-up
-- 1 : GA0 tied to GND (by the VME64X backplane).
-- bit 1 : (RO) - Status of VME P1 signal GA1 (pin P1.D11)
-- 0 : GA1 pull-up
-- 1 : GA1 tied to GND (by the VME64X backplane).
-- bit 2 : (RO) - Status of VME P1 signal GA2 (pin P1.D13)
-- 0 : GA2 pull-up
-- 1 : GA2 tied to GND (by the VME64X backplane).
-- bit 3 : (RO) - Status of VME P1 signal GA3 (pin P1.D15)
-- 0 : GA3 pull-up
-- 1 : GA3 tied to GND (by the VME64X backplane).
-- bit 4 : (RO) - Status of VME P1 signal GA4 (pin P1.D17)
-- 0 : GA4 pull-up
-- 1 : GA4 tied to GND (by the VME64X backplane).
-- bit 5 : (RO) - Status of VME P1 signal GAP (pin P1.D9)
-- 0 : GAP pull-up
-- 1 : GAP tied to GND (by the VME64X backplane).
-- bit 6 : (RO) - Read as '0'.
-- bit 7 : (RO) - Read as '0'.
-- --
-- Encoding table for the GAx register bits .
-- GAP GA4 GA3 GA2 GA1 GA0 slot ID
-- 0 0 0 0 0 1 0x01 -> 1
-- 0 0 0 0 1 0 0x02 -> 2
-- 1 0 0 0 1 0 0x23 -> 3
-- 0 0 0 1 0 0 0x04 -> 4
-- 1 0 0 1 0 1 0x25 -> 5
-- 1 0 0 1 1 0 0x26 -> 6
-- 0 0 0 1 1 1 0x07 -> 7
-- 0 0 1 0 0 0 0x08 -> 8
-- 1 0 1 0 0 1 0x29 -> 9
-- 1 0 1 0 1 0 0x2a -> 10
-- 0 0 1 0 1 1 0x0b -> 11
-- 1 0 1 1 0 0 0x2c -> 12
-- 0 0 1 1 0 1 0x0d  -> 13
-- 0 0 1 1 1 0 0x0e  -> 14
-- 1 0 1 1 1 1 0x2f  -> 15
-- 0 1 0 0 0 0 0x10  -> 16
-- 1 1 0 0 0 1 0x31  -> 17
-- 1 1 0 0 1 0 0x32  -> 18
-- 0 1 0 0 1 1 0x13  -> 19
-- 1 1 0 1 0 0 0x34  -> 20
-- 0 1 0 1 0 1 0x15  -> 21
-- 0 0 0 0 0 0 0x00  -> No VME64X compliant
-- other values are illegal (symptom of a problem)
-- --------------------------------------------------
-- FPGA register : offset 0x03
-- Description : VME reset control/status
-- Width : 8-bit
-- Vector name : fpga_reg(3,i)
-- --------------------------------------------------
-- Description
-- bit 0 : (RO) - Status of the Jumper JP1700
-- 0 : The jumper is OFF and the board set in auto-sensing mode.
-- 1 : The jumper is ON and the board set as system controller.
-- bit 1 : (RO) - Status of the Jumper JP1800
-- 0 : The jumper is OFF and the board CANNOT transmit a reset on
-- the VME.
-- 1 : The jumper is ON and the board CAN assert a reset on the VME.
-- bit 2 : (RO) - Status of the Jumper JP1900
-- 0 : The jumper is OFF and the board CANNOT receive a reset from
-- the VME.
-- 1 : The jumper is ON and the board COULD be reset by the VME.
-- (see also programmable bit fpga_reg(3,4) below.)
-- bit 3 : (RO) - Status of the Universe controller
-- 0 : The Universe is NOT the VME system controller.
-- 1 : The Universe is currently the VME system controller.
-- bit 4 : (RW) - Programmable incoming VME reset enable bit.
-- 0 : A reset on the VME bus cannot reset the board.
-- 1 : A reset on the VME bus COULD reset the board, assuming
-- bit fpga_reg(3,2) is also set to 1.
-- Upon power-up of the VME backplane, this bit is cleared.
-- and remains unchanged upon Front panel reset assertion.
-- bit 5 : (RW) - Programmable enable bit for the Universe local
-- LRST signal.
-- 0 : Will prevent the Universe from propagating a reset to the
-- IIIi board thru the Lrst (pin R1) signal.
-- 1 : Will allow the Universe to propagate a reset into the IIIi
-- board thru the Lrst (pin R1) signal.
-- Upon power-up of the VME backplane, this bit is cleared.
-- and remains unchanged upon Front panel reset assertion.
-- bit 6 : (RW) - reserved for future use
-- Upon power-up of the VME backplane, this bit is cleared.
-- bit 7 : (RW) - Programmable overtemp reset release enable bit
-- 0 : overtemp reset is not release, i.e power cycle is needed.
-- 1 : overtemp reset is release, i.e auto reboot.
-- FPGA register : offset 0x04
-- Description : Temperature sensor status register
-- Width : 8-bit
-- Vector name : fpga_reg(4,i)
-- ----------------------------------
-- Description
-- bit 0 : (RO) - Status of the CPU0 board over-temperature sensor.
-- 0 : No over-temperature condition detected.
-- 1 : Over-temperature condition detected.
-- bit 1 : (RO) - Status of the CPU1 board over-temperature sensor.
-- 0 : No over-temperature condition detected.
-- 1 : Over-temperature condition detected.
-- bit 2 : (RO) - Status of the system board over-temperature sensor.
-- 0 : No over-temperature condition detected.
-- 1 : Over-temperature condition detected.
-- bit 3 : (RO) - Status of the Over-temperature detection log bit;
-- 0 : No over-temperature condition has been detected
-- since the last power-cycling of the VME chassis.
-- 1 : An over-temperature condition has been detected
-- since the last power-cycling of the VME chassis.
-- This bit is reset only when the power is cycled on the
-- VME chassis.
-- bit 3 : (RO) - Status of the Over-temperature detection log bit;
-- 0 : No over-temperature detected since last power cycle.
-- 1 : Occurence of an over-temperature condition has been detected
-- bit 4 : (RO) - Status of the CPU0 board warning temperature indicator.
-- 0 : Temperature below the warning threshold.
-- 1 : Temperature ABOVE the warning threshold.
-- bit 5 : (RO) - Status of the CPU1 board warning temperature sensor.
-- 0 : Temperature below the warning threshold.
-- 1 : Temperature ABOVE the warning threshold.
-- bit 6 : (RO) - Status of the system board warning temperature sensor.
-- 0 : Temperature below the warning threshold.
-- 1 : Temperature ABOVE the warning threshold.
-- bit 7 : (RO) - Over-temperature flag
-- 0 : Temperature below critical threshold.
-- 1 : Temperature rised above critical threshold and still above warning
-- threshold.
-- ----------------------------------
-- FPGA register : offset 0x05
-- Description : miscellaneous & patch control/status register
-- Width : 8-bit
-- Vector name : fpga_reg(5,i)
-- ----------------------------------
-- Description
-- bit 0 : (RO) - OBP flash status bit
Themis Computer

-- 0 : The OBP flash is busy executing a programming command in progress.
-- 1 : The OBP flash is ready to accept a new command.
-- bit 1 : (RW) - This bit controls the System LED
-- 0 : turn-off the System LED.
-- 1 : turn-on the System LED.
-- Upon board reset, the LED is turned-off.
-- bit 2 : (RO) - User flash status bit
-- 0 : The User flash is busy executing a programming command in progress.
-- 1 : The User flash is ready to accept a new command.
-- bit 3 : (RO) - Status of the MXA bus multiplexer control signal.
-- 0 : The MXA bus is used to drive the JTAG bus and is isolate from the XA bus.
-- (Jumper JP2501 installed)
-- 1 : The MXA bus is connected to the XA bus. (Jumper JP2501 removed)
-- 0 : The jumper is installed.
-- 1 : The jumper is removed.
-- Those jumpers are used to set a "patch" number.
-- The generic IIIi will have those three jumpers installed.
-- bit 7 : (RO) - Status of the jumper JP2607
-- 0 : The jumper is removed
-- 1 : The jumper is installed

-------------------
-- FPGA register : offset 0x06
-- Description : SCSI termination status register
-- Width : 8-bit
-- Vector name : fpga_reg(6,i)
-- -------------------
-- Description
-- bit 0 : (RO) - 0 : NO SCSI peripheral has been plugged on the Front panel SCSI A connector.
-- 1 : A SCSI device has been plugged into the front panel SCSI A connector.
-- bit 1 : (RO) - 0 : NO SCSI peripheral has been plugged on SCSI A thru the VME P2 interface.
-- 1 : A SCSI device has been plugged on the SCSI-A bus thru the VME P2 interface.
-- bit 2 : (RO) - 0 : The lower section of the SCSI-A front panel termination is disabled.
-- 1 : The lower section of the SCSI-A front panel termination is enabled.
-- Lower section : SCSI control lines and SCSI data lines [0..7].
-- bit 3 : (RO) - 0 : The upper section of the SCSI-A front panel termination is disabled.
-- 1 : The upper section of the SCSI-A front panel termination is enabled.
-- Upper section : SCSI data lines [8..15].
-- bit 4 : (RO) - 0 : The lower section of the SCSI-A P2 termination is disabled.
-- 1 : The lower section of the SCSI-A P2 termination is enabled.
-- bit 5 : (RO) - 0 : The upper section of the SCSI-A P2 termination is disabled.
-- 1 : The upper section of the SCSI-A P2 termination is enabled.
-- bit 6 : (RO) - Status of the solder bead SB3701 used to indicate what kind of termination devices are used on the Dallas-Sysio board.
-- 0 means UNITRODE UCC5673. SB3701 installed.
-- 1 means Dallas DS2119. SB3701 removed.
-- bit 7 : (RO) - Status of the jumper JP2101 used to force the single-ended mode on
-- SCSI-A.
-- 0 means SCSI-A set in LVD mode. Jumper JP2101 set to 2-3

-- FPGA register : offset 0x07
-- Description : KBM, USB, TTY-A, TTY-B physical port setting
-- Width : 8-bit
-- Vector name : fpga_reg(7,i)
-- ------------------------------
-- Description
-- bit [1..0] : (RO) - These bits provide infos on the setting of the PS/2 and USB
-- Case of DIN8 connector
-- 0 1 : PS/2 on Front - No USB
-- 1 1 : PS/2 on P2 - No USB
-- 1 0 : PS/2 on P2 - USB on the front
-- 0 0 : No PS/2 - USB on the front
-- Case of USB connector
-- 0 1 : No PS/2 - USB on the front
-- 1 1 : PS/2 on P2 - USB on the front
-- 1 0 : PS/2 on P2 - USB on the front
-- 0 0 : No PS/2 - USB on the front
-- bit 1 : (RO) - is the status of the solder bead SB12201.
-- When the solder-bead is set to 2-3, this bit is set to '0'
-- When the solder-bead is set to 1-2, this bit is set to '1'
-- bit 0 : (RO) - is the status of the solder bead SB2105.
-- When the solder-bead is set to 2-3, this bit is set to '1'
-- When the solder-bead is set to 1-2, this bit is set to '0'
-- bit 2 : (RO) - Read as '0'
-- bit 3 : (RO) - 0 : The USB power IC (U12202 - TPS2402) does not report a power failure.
-- 1 : The USB power IC (U12202 - TPS2402) reports a power failure.
-- bit 4 : (RO) - Status of JP2500 which controls the RTC flush mode.
-- 0 : The RTC is operational : jumper JP2500 is OFF.
-- 1 : The RTC is flushed : jumper JP2500 is ON.
-- bit 5 : (RO) - Status of the jumper JP2402 which controls the TTY B port front panel versus P2
-- 0 : The TTY B port is accessible on the front panel.
-- The jumper JP2402 is OFF.
-- 1 : The TTY B port is accessible on VME P2 connector.
-- The jumper JP2402 is ON.
-- bit 6 : (RO) - Status of the jumper JP2401 which controls the
TTY A port front panel versus P2
-- 0 : The TTY A port is accessible on the front panel
-- The jumper JP2401 is OFF.
-- 1 : The TTY A port is accessible on VME P2 connector.
-- The jumper JP2401 is ON.
-- bit 7 : (RO) - Status of the jumper JP2102 which controls the
AC97 port on PMC carrier or on P2
-- 0 : The AC97 Audio port is accessible on the PMC carrier
-- The jumper JP2102 is OFF.
-- 1 : The AC97 Audio port is accessible on VME P2 connector.
-- The jumper JP2102 is ON.
-- ----------------------------------
-- FPGA register : offset 0x08
-- Description : SCSI_A termination control register
-- Width : 8-bit
-- Vector name : fpga_reg(8,i)
-- ----------------------------------
-- Description
-- bit [1..0] : (RW) - These bits control the SCSI-A lower section
of the Front panel termination
-- (SCSI-A control signals and SCSI-A data lines [0..7])
-- 0 0 => The termination are forced in the "disabled" state.
-- 0 1 => The termination are forced in the "enabled" state.
-- 1 X => The termination setting depends on the state of the
  corresponding
-- sense pins.
-- Upon reset, those bits are set to '1'.
-- bit [3..2] : (RW) - These bits control the SCSI-A upper section
of the Front panel termination
-- (SCSI-A data lines [8..15])
-- 0 0 => The termination are forced in the "disabled" state.
-- 0 1 => The termination are forced in the "enabled" state.
-- 1 X => The termination setting depends on the state of the
  corresponding
-- sense pins.
-- Upon reset, those bits are set to '1'.
-- bit [5..4] : (RW) - These bits control the SCSI-A lower section
of the P2 termination
-- (SCSI-A control signals and SCSI-A data lines [0..7])
-- 0 0 => The termination are forced in the "disabled" state.
-- 0 1 => The termination are forced in the "enabled" state.
-- 1 X => The termination setting depends on the state of the
  corresponding
-- sense pins.
-- Upon reset, those bits are set to '1'.
-- bit [7..6] : (RW) - These bits control the SCSI-A upper section
of the P2 termination
-- (SCSI-A data lines [8..15])
-- 0 0 => The termination are forced in the "disabled" state.
-- 0 1 => The termination are forced in the "enabled" state.
-- 1 X => The termination setting depends on the state of the corresponding sense pins.
-- Upon reset, those bits are set to '1'.
-- -----------------------------------------------------
-- FPGA register : offset 0x09
-- Description : SCSI-A/B termination power control and User switch setting
-- Width : 8-bit
-- Vector name : fpga_reg(9,i)
-- -----------------------------------------------------
-- Description
-- bit 0 : (RW) - Control the termination power on SCSIA.
-- 0 : The termination power on SCSI-A is enabled.
-- 1 : The termination power on SCSI-A is shutdown.
-- bit 1 : (RW) - Control the termination power on SCSIB.
-- 0 : The termination power on SCSI-B is enabled.
-- 1 : The termination power on SCSI-B is shutdown.
-- bit 2 : (RO) - Status of the sense pin on the SCSI-B interface.
-- 0 : NO scsi device plugged onto SCSI-B interface
-- 1 : a SCSI device is plugged onto SCSI-B interface
-- bit 3 : (RO) - Read as '0'
-- bit [7..4] : (RO) - User switch value
-- register value 0xf when the rotary switch is set in position 0
-- register value 0xe when the rotary switch is set in position 1
-- ....
-- register value 0x3 when the rotary switch is set in position 12
-- register value 0x2 when the rotary switch is set in position 13
-- register value 0x1 when the rotary switch is set in position 14
-- register value 0x0 when the rotary switch is set in position 15
-- positions E,F are reserved for the following situation
-- positions E,F : OBP/POST from the recovery PROM. Reserved for Themis use.
-- other positions : OBP/POST source defined by JP2502
-- (OFF=recovery , ON = Normal)
-- -----------------------------------------------------
-- FPGA register : offset 0x0a
-- Description : JTAG register
-- Width : 8-bit
-- Vector name : fpga_reg(10,i)
-- -----------------------------------------------------
-- Description
-- This register is used to program the EPC2 Eeprom.
-- bit 0 : (RW) - JTAG TMS signal ( 0 means asserted low, 1 means asserted high)
-- Upon board reset, TMS signal is asserted low.
-- bit 1 : (RW) - JTAG TRST signal ( 0 means asserted low, 1 means asserted high)
Upon board reset, TRST signal is asserted low.

bit 2: (RW) - JTAG TCK signal (0 means asserted low, 1 means asserted high)

Upon board reset, TCK signal is asserted low.

bit 3: (RW) - JTAG TDI signal (0 means asserted low, 1 means asserted high)

Upon board reset, TDI signal is asserted low.

The name TDI refers to the EPC2 component. TDI is an input for
the EPC2 and therefore must be an output from the FPGA

bit 4: (RO) - JTAG TDO signal (0 means asserted low, 1 means asserted high)

The name TDO refers to the EPC2 component. TDO is an output for
the EPC2 and therefore must be an input to the FPGA

bit 5: (RO) - An over-temperature condition has been detected on CPU0

bit 6: (RO) - An over-temperature condition has been detected on CPU1

bit 7: (RO) - An over-temperature condition has been detected on CPU2

FPGA register: offset 0x0b

Description: Fibre Channel / GBE Status register

Width: 8-bit

Vector name: fpga_reg(11,i)

Description:

bit 0: (RW) - Redirect i2c SCL Xver signal to FC1 GBIC transceiver

bit 1: (RW) - Transmit disable on Fibre Channel #1

bit 2: (RW) - Redirect i2c SCL Xver signal to FC2 GBIC transceiver

bit 3: (RW) - Transmit disable on Fibre Channel #2

bit 4: (RW) - Redirect i2c SCL Xver signal to GBE1 GBIC transceiver

bit 5: (RW) - Transmit disable on GBE Channel #1

bit 6: (RW) - Redirect i2c SCL Xver signal to GBE2 GBIC transceiver

bit 7: (RW) - Transmit disable on GBE Channel #2

FPGA register: offset 0x0c

Description: User flash Ebus low address diagnostic register

Width: 8-bit

Vector name: fpga_reg(12,i)

Description:

bit [7..0]: (RO) - previous Ebus address [7..0]

FPGA register: offset 0xd

Description: Ebus medium address diagnostic register

Width: 8-bit
Vector name : fpga_reg(13,i)
----------------------------------
-- Description
-- bit [7..0] : (RO) - previous Ebus address [15..8]
-- ----------------------------------
-- FPGA register : offset 0x0e
-- Description : Ebus high address diagnostic register
-- Width : 8-bit
-- Vector name : fpga_reg(14,i)
-- ----------------------------------
-- Description
-- bit [7..0] : (RO) - previous Ebus address [23..16]
-- ----------------------------------
-- FPGA register : offset 0x0f
-- Description : scratchpad register
-- Width : 8-bit
-- Vector name : fpga_reg(15,i)
-- ----------------------------------
-- Description
-- scratch register used to speed up the programming of the FPGA :
-- bit 0 = TMS output signal alias of bit fpga_reg(10,0)
-- bit 1 = TDI output signal alias of bit fpga_reg(10,3)
-- bit 7..2 = Count value . How many times we want to send the pattern
-- set on bit[1..0] onto the JTAG interface.
4.1 Introduction

The USPIIIi-OPT design contains two categories of monitoring devices:

- Thermal measurement
- DC/DC converter voltage measurement

4.2 Thermal Monitoring

USPIIIi-OPT thermal sensors are all based on the I²C ADM1031 from Analog Devices. There are a total of three thermal sensors, one on each major board of the USPIIIi-OPT; namely, the System board, the CPU-0 board, and the CPU-1 board.

Each ADM1031 sensor is able to report three temperatures: the first temperature is that of the ADM1031 device itself; the second and third temperatures are those of the two remote diodes used as sensors.

On both the CPU-0 and CPU-1 boards, one of the diodes is on the CPU die; therefore its temperature can be considered the CPU junction temperature. The second diode is a discrete component placed on the board in a location that is given in Figure 4-1 on page 4-2.

On the System board, the two remote diodes are discrete components, one placed at the inlet, the other at the exhaust. Their location is provided in details in Figure 4-1.
Figure 4-1. Placement of USPIIIi-OPT Device Monitors
The temperature sensor controller ADM1031 provides two outputs. One (THERM) is asserted to report the temperature has risen above the warning threshold, called Therm-limit in the ADM1031 datasheet, and is deasserted when the temperature reaches a full 5°C below the Therm-limit threshold.

The other (INT or SMBALERT) is asserted when the temperature is out of the programmable temperature low and high thresholds.

The behavior of these two signals is pictured (in a simplistic way) in Figure 4-2.

![Figure 4-2. Outputs of the Temperature Sensor Controller](image-url)
4.2.1 Setting Temperature Thresholds

The following environment variables are used to set the temperature thresholds for the three sensors:

- `system-low-limit` 0
- `system-therm-limit` 80
- `system-high-limit` 70
- `cpu1-low-limit` 5
- `cpu1-therm-limit` 105
- `cpu1-high-limit` 100
- `cpu0-low-limit` 5
- `cpu0-therm-limit` 105
- `cpu0-high-limit` 100

To change the temperature threshold, type:

```bash
{1} ok setenv system-therm-limit 85
```

To see the current temperature reading on the different sensors type:

```bash
{1} ok .env
```

```
System Board

<table>
<thead>
<tr>
<th>Sensor</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inlet</td>
<td>+27 C</td>
</tr>
<tr>
<td>Outlet</td>
<td>+46 C</td>
</tr>
<tr>
<td>Local</td>
<td>+39 C</td>
</tr>
</tbody>
</table>

CPU 0

<table>
<thead>
<tr>
<th>Sensor</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die</td>
<td>+86 C</td>
</tr>
<tr>
<td>Board Sensor</td>
<td>+63 C</td>
</tr>
<tr>
<td>Local</td>
<td>+47 C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage Source</th>
<th>Input Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ain0 (Backplane +5V)</td>
<td>4980 mV</td>
</tr>
<tr>
<td>Ain1 (Memory +2.5V)</td>
<td>2578 mV</td>
</tr>
<tr>
<td>Ain2 (Jbus +1.5V)</td>
<td>1503 mV</td>
</tr>
<tr>
<td>Ain3 (CPU core +Vcore)</td>
<td>1386 mV</td>
</tr>
</tbody>
</table>

CPU 1

<table>
<thead>
<tr>
<th>Sensor</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die</td>
<td>+78 C</td>
</tr>
<tr>
<td>Board Sensor</td>
<td>+49 C</td>
</tr>
<tr>
<td>Local</td>
<td>+33 C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage Source</th>
<th>Input Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ain0 (Backplane +5V)</td>
<td>4980 mV</td>
</tr>
<tr>
<td>Ain1 (Memory +2.5V)</td>
<td>2578 mV</td>
</tr>
<tr>
<td>Ain2 (Jbus +1.5V)</td>
<td>1484 mV</td>
</tr>
<tr>
<td>Ain3 (CPU core +Vcore)</td>
<td>1386 mV</td>
</tr>
</tbody>
</table>
```
To see a more detailed listing of the sensor temperatures and their threshold settings:

```bash
{1} ok themis-show-temp
System Board Temperature

I2C address :      58
Device      : ADM1031 (Analog devices)

ADM1031 device ID (0x31)     : 31
Company ID (0x41)            : 41
Revision                     : 3
Remote 1 temperature parameters :
  Temperature High limit :   +70
  Temperature Low limit :    +0
  Temperature THERM limit :  +80
  Temperature                --> Remote 1 :    +27

Remote 2 temperature parameters :
  Temperature High limit :   +70
  Temperature Low limit :    +0
  Temperature THERM limit :  +80
  Temperature                --> Remote 2 :    +45

Local temperature parameters :
  Temperature High limit :   +70
  Temperature Low limit :    +0
  Temperature THERM limit :  +80
  Temperature                --> local :    +39

CPU0 Temperature

I2C address :      5c
Device      : ADM1031 (Analog devices)

ADM1031 device ID (0x31)     : 31
Company ID (0x41)            : 41
Revision                     : 3
Remote 1 temperature parameters :
  Temperature High limit :   +100
  Temperature Low limit :    +5
  Temperature THERM limit :  +105
  Temperature                --> Remote 1 :    +86

Remote 2 temperature parameters :
  Temperature High limit :  +100
  Temperature Low limit :    +5
```
Temperature THERM limit :   +105
Temperature   ----->     Remote 2 :    +63

Local temperature parameters :
  Temperature High limit :   +70
  Temperature Low limit :   +0
  Temperature THERM limit :   +80
Temperature   ----->     local :    +47

CPU1 Temperature

-------------
I2C address :      5e
Device      : ADM1031 (Analog devices)

ADM1031 device ID (0x31)     : 31
Company ID (0x41)            : 41
Revision                     : 3

Remote 1 temperature parameters :
  Temperature High limit :   +100
  Temperature Low limit :   +5
  Temperature THERM limit :   +105
    Temperature   ----->     Remote 1 :    +78

Remote 2 temperature parameters :
  Temperature High limit :   +100
  Temperature Low limit :   +5
  Temperature THERM limit :   +105
    Temperature   ----->     Remote 2 :    +49

Local temperature parameters :
  Temperature High limit :   +70
  Temperature Low limit :   +0
  Temperature THERM limit :   +80

Under Solaris, you can dump the temperature of the different sensors using the following command:

# ./usp3iopt_temp
System Board :  config1 = 0x01   config2 = 0x70
CPU0         :  config1 = 0x81   config2 = 0x70
System Board :  status1 = 0x00  status2 = 0x00
CPU0         :  status1 = 0x00  status2 = 0x00
Sys local   temperature is   28
  Therm limit:   80
  High limit :    70
  Low limit :     0
Sys inlet temperature is 29
  Therm limit: 80
  High limit : 70
  Low limit : 0
Sys outlet temperature is 33
  Therm limit: 80
  High limit : 70
  Low limit : 0
CPU-0 local temperature is 34
  Therm limit: 80
  High limit : 70
  Low limit : 0
CPU-0 die temperature is 59
  Therm limit: 105
  High limit : 100
  Low limit : 5
CPU-0 board temperature is 39
  Therm limit: 105
  High limit : 100
  Low limit : 5
CPU-1 local temperature is 34
  Therm limit: 80
  High limit : 70
  Low limit : 0
CPU-1 die temperature is 77
  Therm limit: 105
  High limit : 100
  Low limit : 5
CPU-1 board temperature is 49
  Therm limit: 105
  High limit : 100
  Low limit : 5

#

You can also change the thresholds by typing "./usp3i_temp -c":

# ./usp3iopt_temp -c
Sys local temperature is 38
  Therm limit: 80
  new value:
Type the new value or simply hit enter to continue without changing.

To run the utility in monitor mode, type:

# ./usp3iopt_temp -m
4.3 Voltage Monitoring

The USPIIIi-OPT CPU-0/CPU-1 boards have many built-in DC/DC converters. The voltage output must be set to very specific values in order to get maximum performance. As a result, it is vital to implement a capability to monitor these critical voltages.

Design of the USPIIIi-OPT contains an I²C A/D converter on each CPU board that allows us to read the current voltage of the many critical DC/DC converters outputs. The voltages monitored are listed in Table 4-1.

<table>
<thead>
<tr>
<th>Table 4-1. Voltages Monitored on the CPU-0 and CPU-1 Boards</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU-0</strong></td>
</tr>
<tr>
<td>VCC (+5V) backplane</td>
</tr>
<tr>
<td>2.5V DDR memory0 voltage</td>
</tr>
<tr>
<td>1.5V Jbus termination voltage</td>
</tr>
<tr>
<td>VCCP0 CPU core voltage</td>
</tr>
</tbody>
</table>

To see the current voltage levels, type the OBP command:

```
{1} ok themis-show-voltage
CPU0 Voltage
--------
Voltage on Ain0 (Backplane +5V ) input : 4980 mV
Voltage on Ain1 (Memory +2.5V ) input : 2578 mV
Voltage on Ain2 (Jbus +1.5V ) input : 1503 mV
Voltage on Ain3 (CPU core +Vcore) input : 1367 mV
CPU1 Voltage
--------
Voltage on Ain0 (Backplane +5V ) input : 4980 mV
Voltage on Ain1 (Memory +2.5V ) input : 2578 mV
Voltage on Ain2 (Jbus +1.5V ) input : 1484 mV
Voltage on Ain3 (CPU core +Vcore) input : 1386 mV
{1} ok
```
Index

A
A/D converter 4-8
ADM1031 datasheet 4-3
ADM1031 device 4-1
ADM1031 sensor 4-3
AMD device AM29LV065D 1-1
Analog voltage I2C converter 1-1

C
CPU junction temperature 4-1
CPU-0 x
CPU-0 board 4-1
CPU-1 x
CPU-1 board 4-1
CY37512 programmable logic device 1-1

D
DC/DC converter 4-1
DC/DC converters 4-8
device monitors 4-2

E
environment variables 2-3
Environmental Monitoring Programs 2-7

F
fiber-channel controller ISP2312 1-1
Field-Programmable Gate Array (FPGA) 3-1
Flash PROM
  updating 2-5
Flash update 2-6
FPGA 3-1
FPGA functions 3-1
  dump-fpga 3-1
  dump-jumper 3-1
Examples 3-2
  pldc! 3-2
  pldc@ 3-2
  pldl! 3-2
  pldl@ 3-2
  pldw! 3-2
  pldw@ 3-2
themis-show-pld 3-1

I
I2C ADM1031 device 4-1
I2C bus topology 1-2
I2C devices address map 1-6
I2C thermal sensor ADM1031 1-1
IDsel assignments 1-2
In Case Of Difficulties xi
INT 4-3
Intended Audience xi
Interrupt assignment/mapping 1-2

J
Jbus 1-2
Jbus Address Map 1-3
Jbus Address Space 1-4
Jbus address space 1-2
Jbus configuration space layout 1-3
Jbus ID assignment 1-3
Jbus topology 1-2
JID 1-2

M
monitoring devices
  thermal measurement 4-1
  voltage measurement 4-1

N
native firmware 1-1
O

OBP
  device aliases 2-2
  Support Commands 2-2
OBP commands, additional 2-3
OBP v4.0 commands 2-1
OBP version 4.0 2-1
Outputs
  Temperature Sensor Controller 4-3

P

PCI Configuration Space 1-4
PCI segments topology 1-2
placement of USPIIIi-OPT device monitors 4-2
PMC Carrier boards x
programming guide 1-1

R

recovery OBP 2-6

S

semaphores 1-1
shared resources 1-1
slot configurations, VME. See VME slot configurations
SMBALERT 4-3
software 2-1
  Environmental Monitoring Programs 2-7
  SUN Solaris Operating System 2-7
  usp3i_temp program 2-7
  usp3i_uled program 2-8
  usp3i_voltage program 2-7
software programming guide 1-1
Solaris 2-7
SPARC version 9.0 ix
Sun native firmware 1-1
SUN Solaris 2-7
System board x, 4-1

T

temperature sensor controller ADM1031 4-3
temperature sensors
  THERM output 4-3
TGA3D/3D+ Graphics board x
THERM output 4-3
Thermal measurement 4-1
thermal sensors 4-1
Tomatillo 1-2, 1-3

U

Universe-II controller 1-1
Updating flash from the recovery OBP 2-6
User LED I2C driver 1-1
usp3i_temp application 2-7
usp3i_uled application 2-8
usp3i_voltage application 2-7
USPIIIi-OPT
  models x
  slot configurations x
  Software 2-1

V

VME P2 Paddle board x
VME slot configurations x
VMEbus interface ix
voltage monitoring 4-8
voltages monitored
  CPU-0 and CPU-1 Boards 4-8

W

warning threshold, temperature 4-3